Please add the following new claims:

24. (New) An arrangement, comprising:

p-doped semiconductor layers;

n-doped semiconductor layers; and

a plurality of transitions arranged between the p-doped semiconductor layers and the n-doped semiconductor layers, the transitions displaying a Zener breakdown upon application of a characteristic voltage for each of the transitions, wherein the characteristic voltages of the transitions additively correspond to a breakdown voltage of the arrangement.

25. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers are highly doped.

26. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers exhibit a constant doping.

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27. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers are doped at a same concentration.

28. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers form at least two groups doped at different concentrations.

29. (New) The arrangement according to claim 24, wherein the n-doped semiconductor layers form at least two groups that are doped at different concentrations.

30. (New) The arrangement according to claim 24, further comprising:

an n-doped substrate on which are arranged the p-doped semiconductor layers and the n-doped semiconductor layers.

31. (New) The arrangement according to claim 30, wherein a doping type of a semiconductor layer farthest away from the n-doped substrate corresponds to a doping type of the n-doped substrate.

32. (New) The arrangement according to claim 30, wherein a doping type of a semiconductor layer farthest away from the n-doped substrate is different than a doping type of the n-doped substrate.

33. (New) The arrangement according to claim 30, wherein the n-doped substrate has a thickness of approximately 500μm.

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34. (New) The arrangement according to claim 24, further comprising:

a p-doped substrate on which are arranged the p-doped semiconductor layers and the n-doped semiconductor layers.

35. (New) The arrangement according to claim 34, wherein a doping type of a semiconductor layer farthest away from the p-doped substrate corresponds to a doping type of the p-doped substrate.

36. (New) The arrangement according to claim 34, wherein a doping type of a semiconductor layer farthest away from the p-doped substrate is different than a doping type of the p-doped substrate.

37. (New) The arrangement according to claim 35, wherein the p-doped substrate has a thickness of approximately 500μm.

38. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers have a thickness of approximately 4μm.

39. (New) The arrangement according to claim 24, wherein a concentration of doping for the p-doped semiconductor layers and the n-doped semiconductor layers is approximately 2×10^{19} atoms/cm^3.

40. (New) The arrangement according to claim 24, wherein ten transitions are provided between the p-doped semiconductor layers and the n-doped semiconductor layers.

41. (New) The arrangement according to claim 24, further comprising:

metal contacts arranged over an entire respective surface of an upper side and a lower side of the arrangement.

42. (New) The arrangement according to claim 24, wherein the n-doped semiconductor layers and the p-doped semiconductor layers are silicon layers.

43. (New) A method to manufacture an arrangement having p-doped semiconductor layers, n-doped semiconductor layers, and transitions arranged between the p-doped semiconductor layers and the n-doped semiconductor layers, the transitions displaying a Zener breakdown upon application of a characteristic voltage for each of the transitions, wherein the characteristic voltages of the transitions additively correspond to a breakdown voltage of the arrangement, the method comprising:

applying the p-doped semiconductor layers and the n-doped semiconductor layers by epitaxy.

44. (New) The method according to claim 43, wherein the epitaxy is applied at approximately 1180°C.

45. (New) The method according to claim 43, wherein the epitaxy is performed at a growth rate of approximately 4 μm/min.

46. (New) The method according to claim 43, further comprising:

sputtering metal contacts onto an upper side and a lower side of the arrangement.

47. (New) The method according to claim 46, further comprising:

after sputtering, dividing the arrangement into individual chips.